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DiGiulio et al.

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[54] **RESET DELAY CIRCUIT FOR AN ELECTRONIC POSTAGE METER**

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[58] **Field of Search** 564/464, 466, 200, 900

[56] **References Cited**

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[57] **ABSTRACT**

An electronic postage meter with a circuit to provide for a delay period before operation of a postage meter is disclosed. The circuit provides a fixed delay which is triggered when three input signals provided to the circuit become active. The input signals will be active in this embodiment to indicate satisfactory regulated voltage level, a satisfactory unregulated voltage level, and a satisfactory external clock frequency respectively. The output of the delay circuit upon acceptance of these active signals provides a reset delay signal to a system processor and also controls the signals that are provided to the non-volatile memories and the system printer. The circuit uses advantageously logic devices to provide the delay of the output signal rather than the traditional utilization of R-C network. The delay circuit is particularly useful in a system such as postage meter that utilizes a microprocessor and a non-volatile memory, to protect the contents of the non-volatile memory.

5 Claims, 11 Drawing Figures